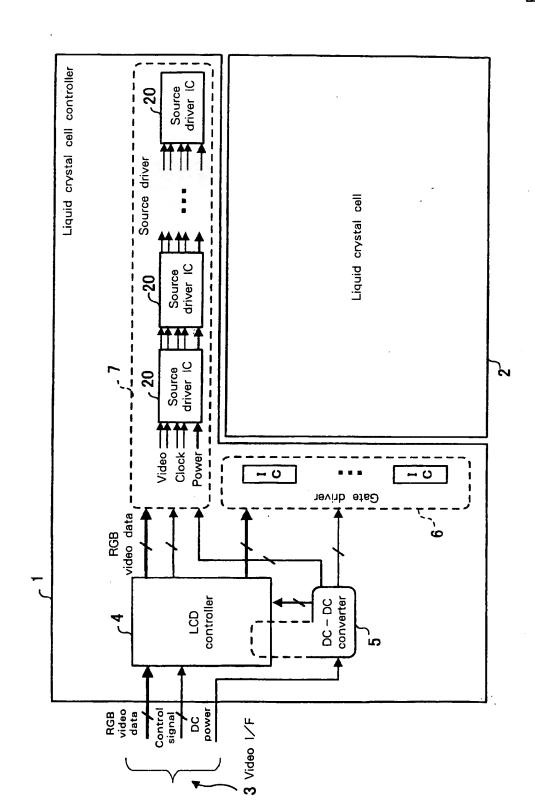
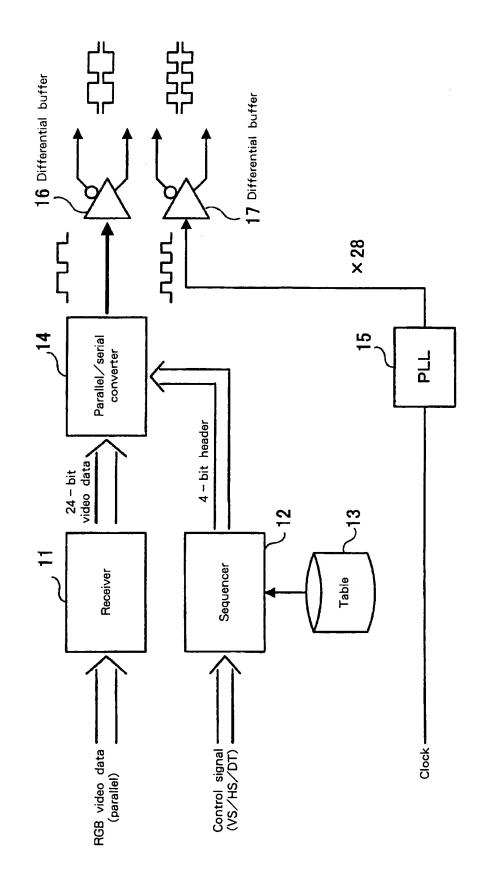
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of the first transition than the second transition and then then than that that the



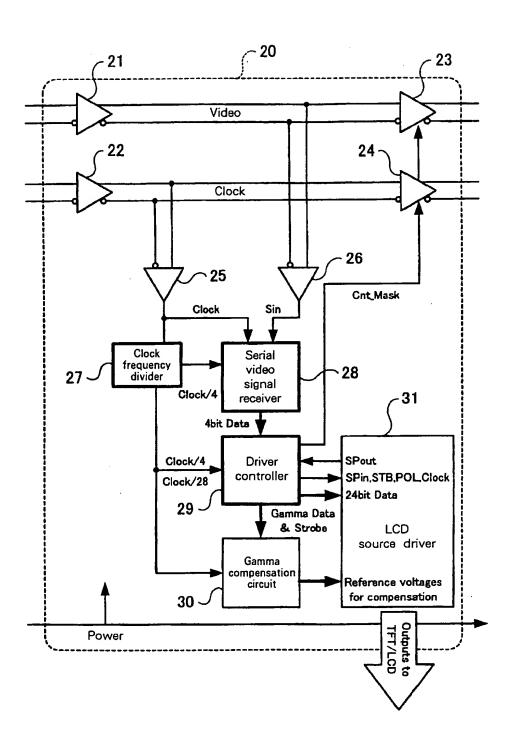
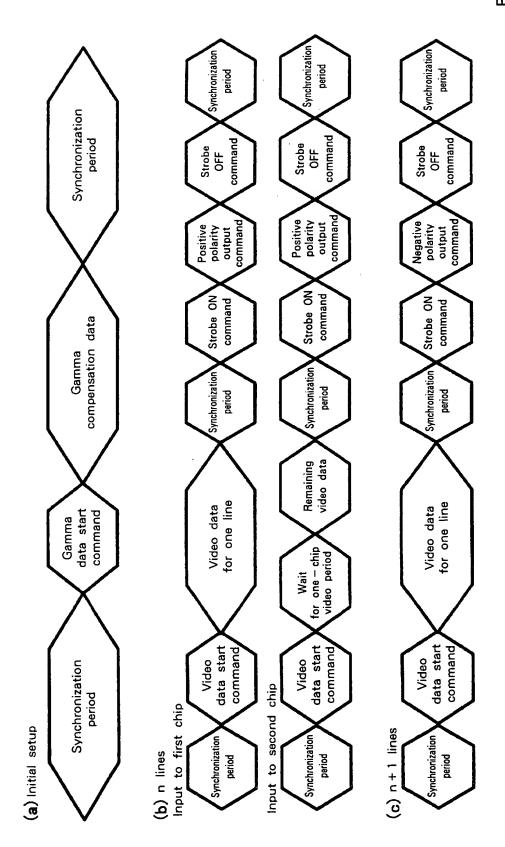


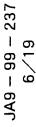
Fig. 3

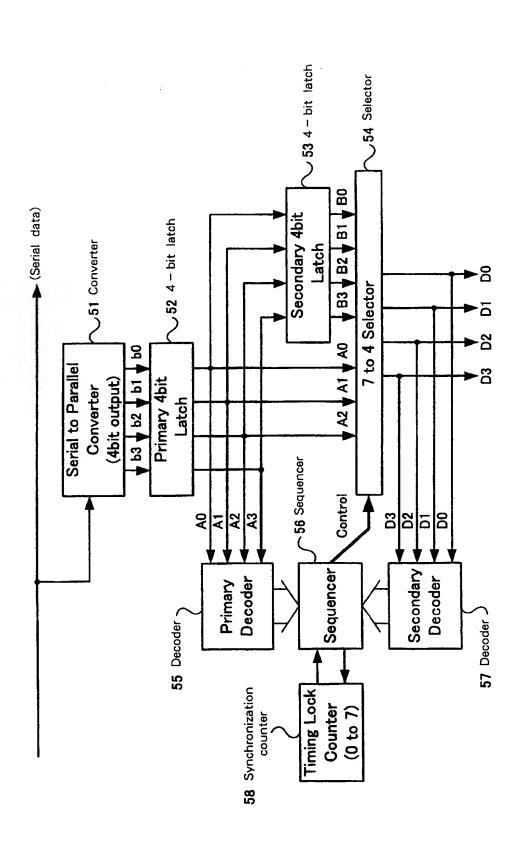
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S 42	Data	All zero	Command bits	Data bits	Undefined
	24bit	[00000000000000000000]	24bit	24bit	24bit
41	Header	Sync	Command	Data	Wait
	4bit	[1000]	[1100]	[1110]	[1111]
	Bit block format	(1) Synchronization bit block	(2) Command bit block	(3) Data bit block 46	(4) Wait bit block

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Parallel output

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4 - bit latch (n clock) [A3, A2, A1, A0]	Selector (n + 1 clock) [D3, D2, D1, D0]	Control ID
[1, 0, 0, 0]	[A2, A1, A0, B3]	0
[0, 1, 0, 0]	[A1, A0, B3, B2]	1
[0, 0, 1, 0]	[A0, B3, B2, B1]	2
[0, 0, 0, 1]	[B3, B2, B1, B0]	3

Fig. 8

Bit block type	Comparison pattern with selector output [D3, D2, D1, D0]		
Synchronization	[0, 0, 0, 1]		
Command	[0, 0, 1, 1]		
Data	[0, 1, 1, 1]		
Wait	[1, 1, 1, 1]		

Fig. 9

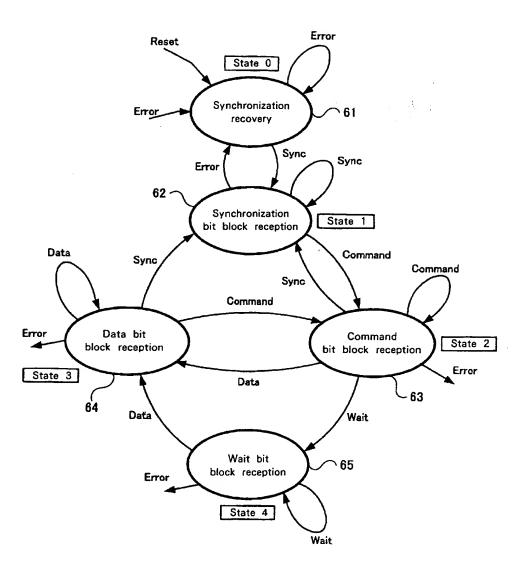
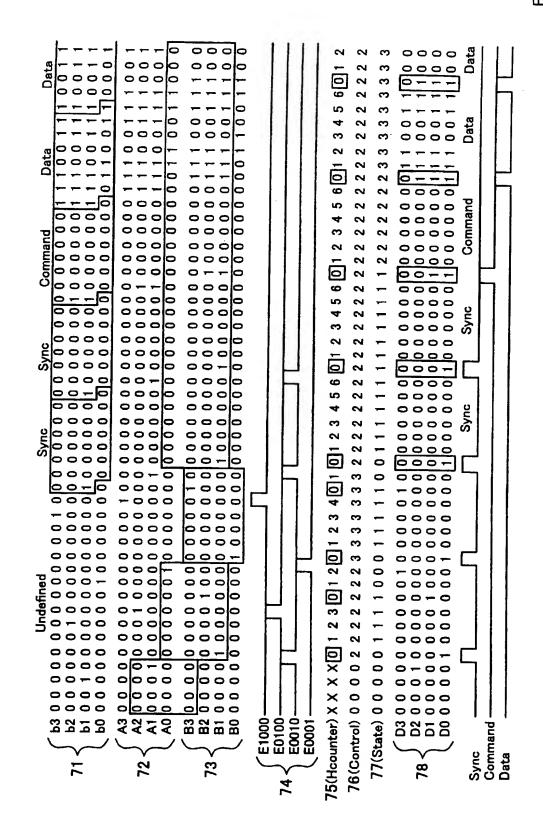


Fig. 10

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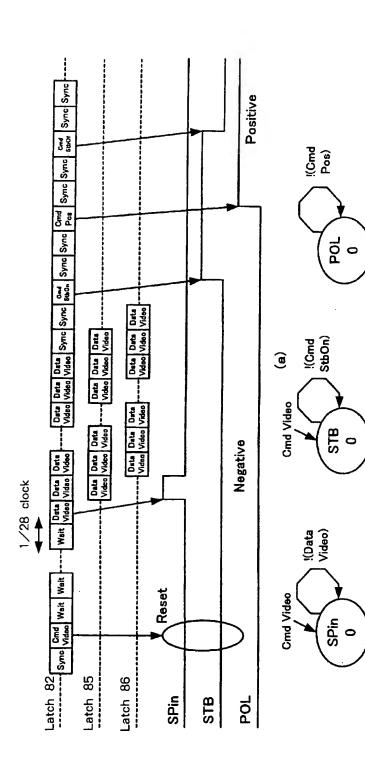


Fig. 13

Cmd Pos

Cmd Neg

Cmd StbOn

Cmd StbOf

Data Video

POL

STB

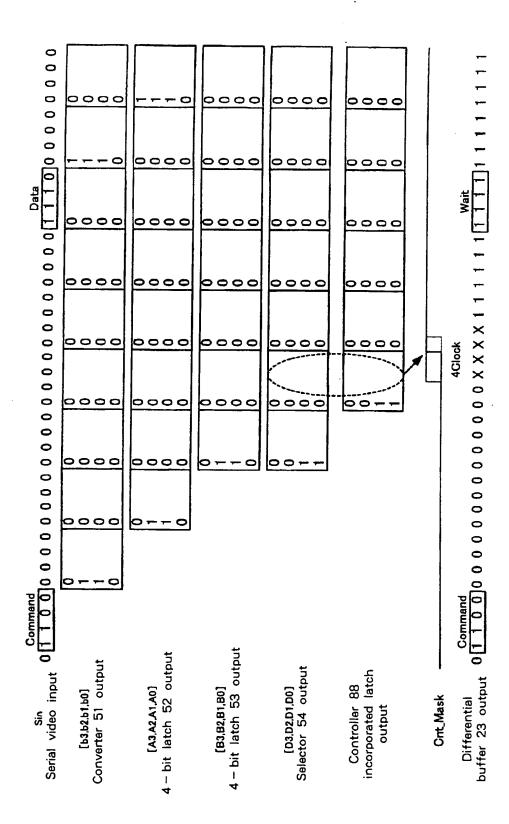
SPin -

!(Cmd Neg)

!(Cmd StbOf)

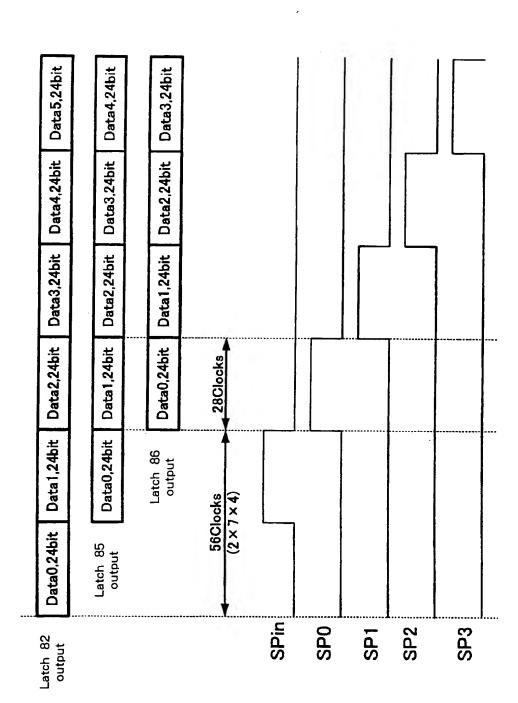
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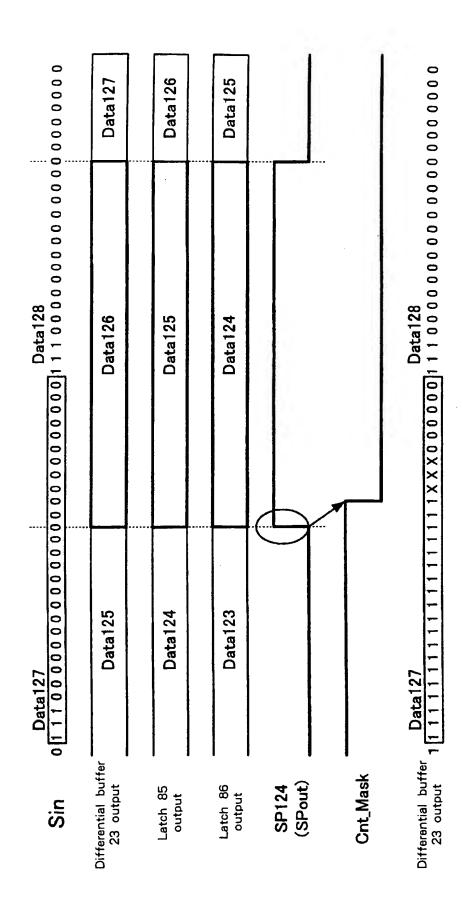


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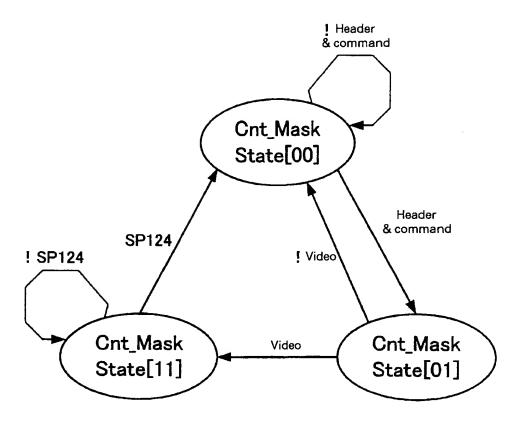
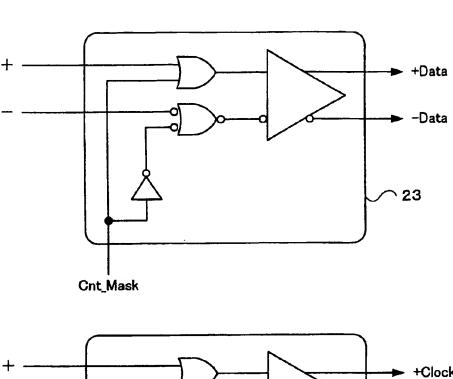


Fig. 18





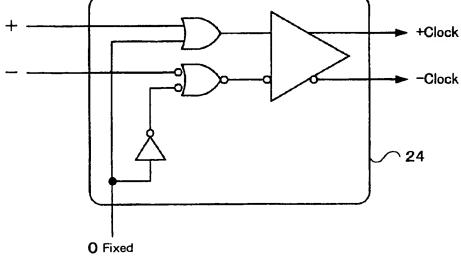


Fig. 19



